**EX.NO: 2 DESIGN ENTRY AND SIMULATION OF SEQUENTIAL LOGIC CIRCUITS**

**DATE:**

**AIM:**

To design and simulate the sequential logic circuits (Flip-flops, Counters & Registers) using Verilog module Xilinx Vivado Webpack.

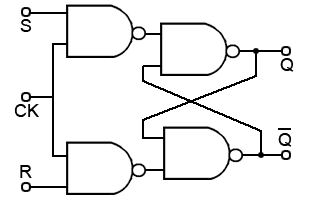
**SOFTWARE REQUIRED:**

Vivado Design Suite WebPACK™ Edition

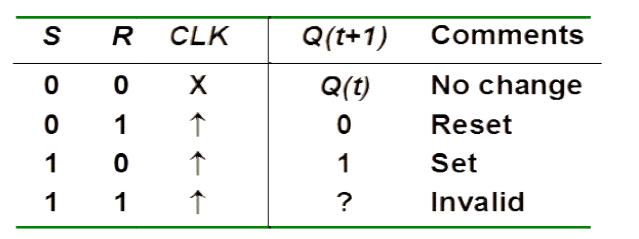
**a) FLIP-FLOPS:**

**(i) SR FLIP-FLOP:**

**Logic Circuit**



**Truth Table**

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**PROGRAM:**

a) GATE LEVEL MODELING:

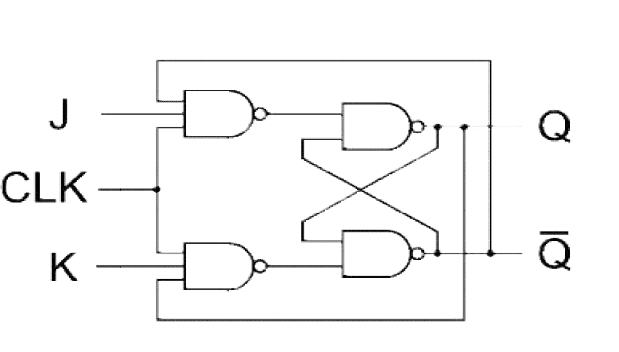
b) DATAFLOW MODELLING:

c) BEHAVIORAL MODELLING:

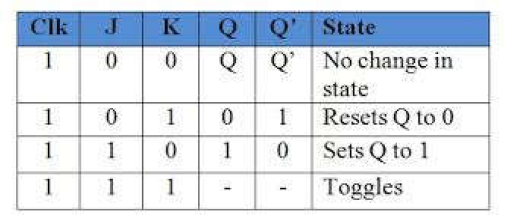
**SIMULATION OUTPUT:**

**(ii) JK FLIP-FLOP:**

**Logic Circuit**

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**Truth Table**

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**PROGRAM:**

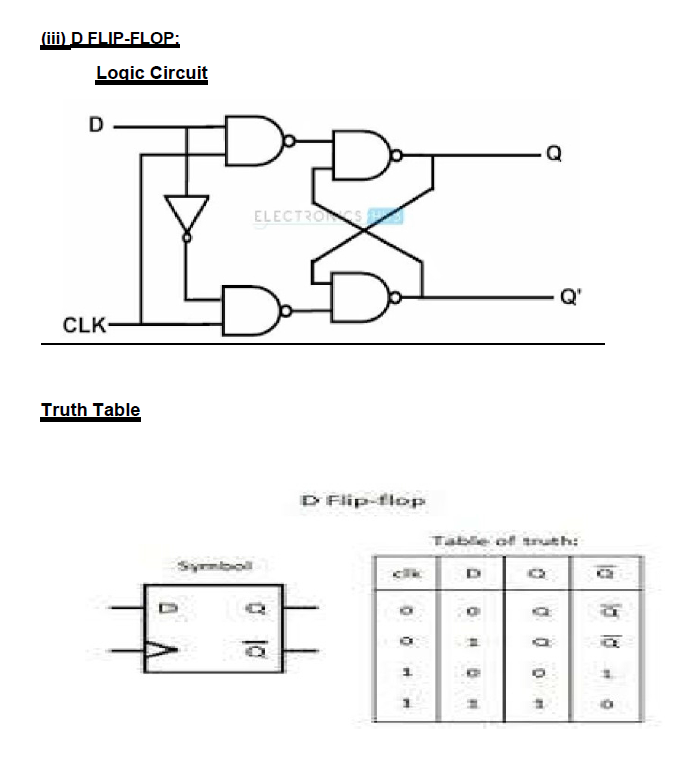
a) GATE LEVEL MODELING:

b) DATAFLOW MODELLING:

c) BEHAVIORAL MODELLING:

**SIMULATION OUTPUT**

**(iii) D flip flop**



**(iv) T-Flip Flop**

